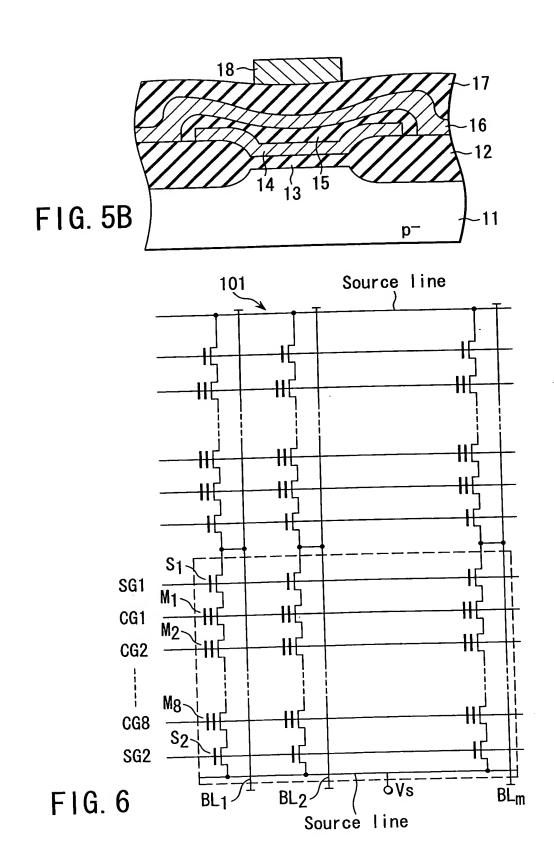
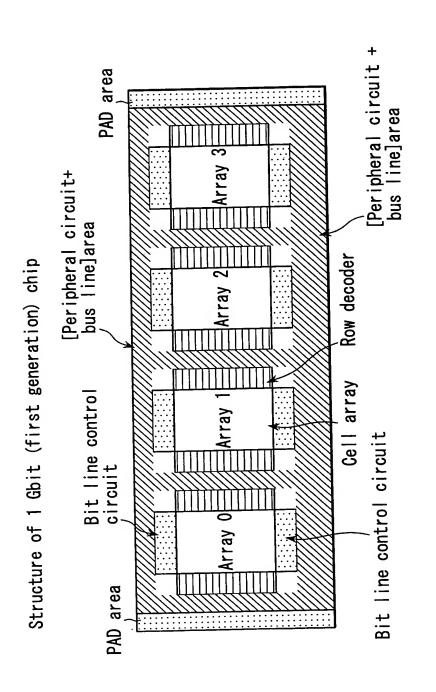


FIG. 5A





F1G. 7

Chip image when package product of FIG. 15 is seen from external device Chip Array3 Array2 address Array1 Array0 = 0"area Chip Array3 address Array2 Arrav0 Array1 = 1"area FIG. 8 Array 3 Array 2 Array 1 Array 0 (corresponding (corresponding (corresponding to Table 2) to Table 2) to Table 2) to Table 2) 2 Gbit package product 2 Gbit package product (second generation product is used) Array3 Array2 Array1 Array0 Array7 Array6 Array5 Array4 Array 3 FIG. 9 Array 1 Array 2 Array 0 (corresponding (corresponding to Table 4) to Table 4) to Table 4)

to Table 4)

to Table 4)

4 Gbit package product (first generation product is used)

A Gbit package product 1 Gbit (first generation) chip

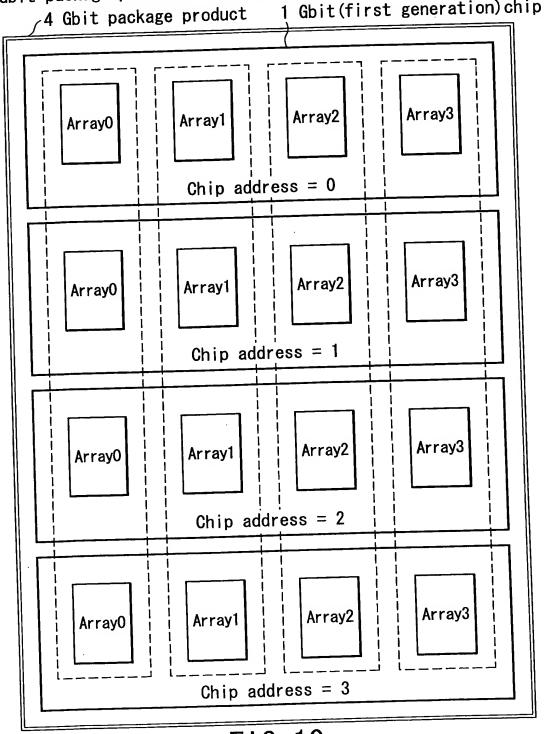


FIG. 10

Gbit package product (second generation product is used)

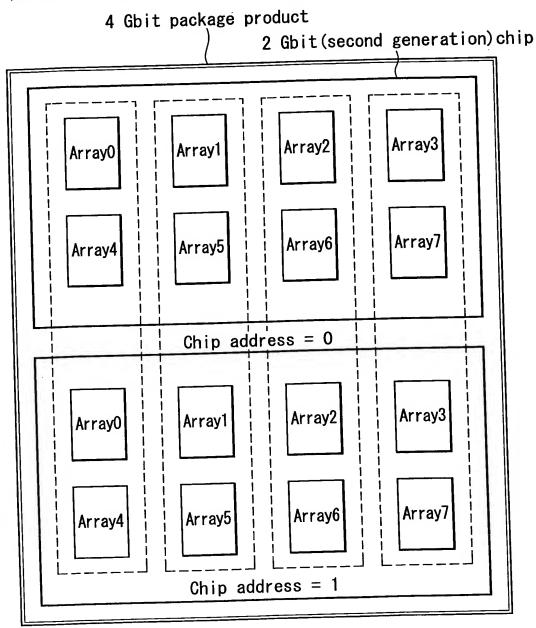


FIG. 11

4 Gbit package product (third generation product is used)

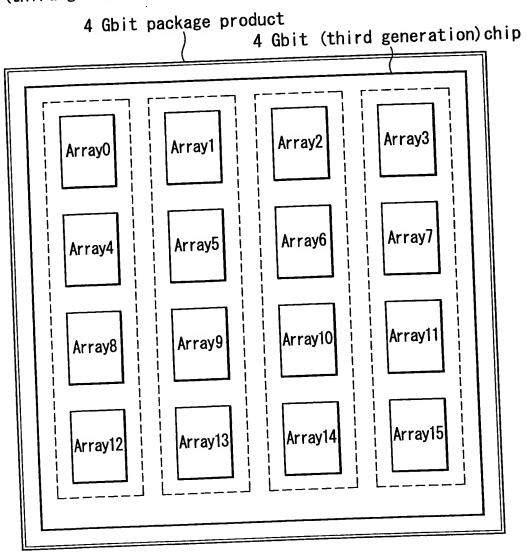


FIG. 12

4 Gbit package product (second generation product is used)

4 Gbit package product 2 Gbit(second generation)chip Array 3 Array 2 Array 1 Array 0 Array 7 Array 6 Array 5 Array 4 Chip address = 0Array 3 Array 2 Array 1 Array O Array 7 Array 6 Array 5 Array 4 Chip address = 1

FIG. 13

"Chip address = 1"area "Chip address = 0"area "Chip address = 1"area "Chip address = 0"area F1G. 14 Chip image when package product of FIG.11 is seen from external device Array Array Array Array Array 2 Array Array Array 4 Gbit package product Array Array Array Array Array Array Array Array

4 Gbit package product (third generation product is used)

Ghit package product

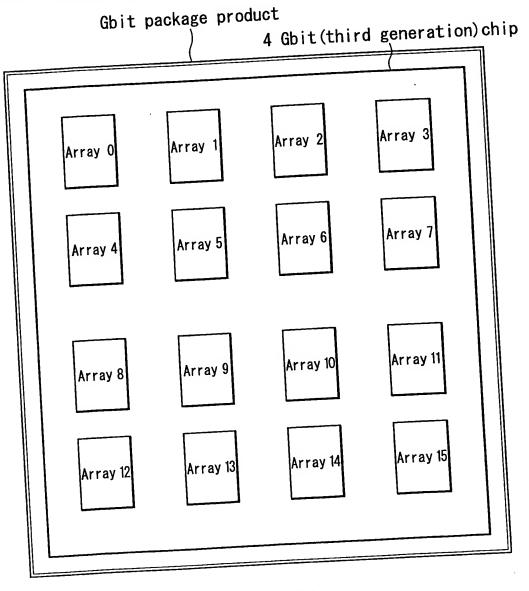


FIG. 15